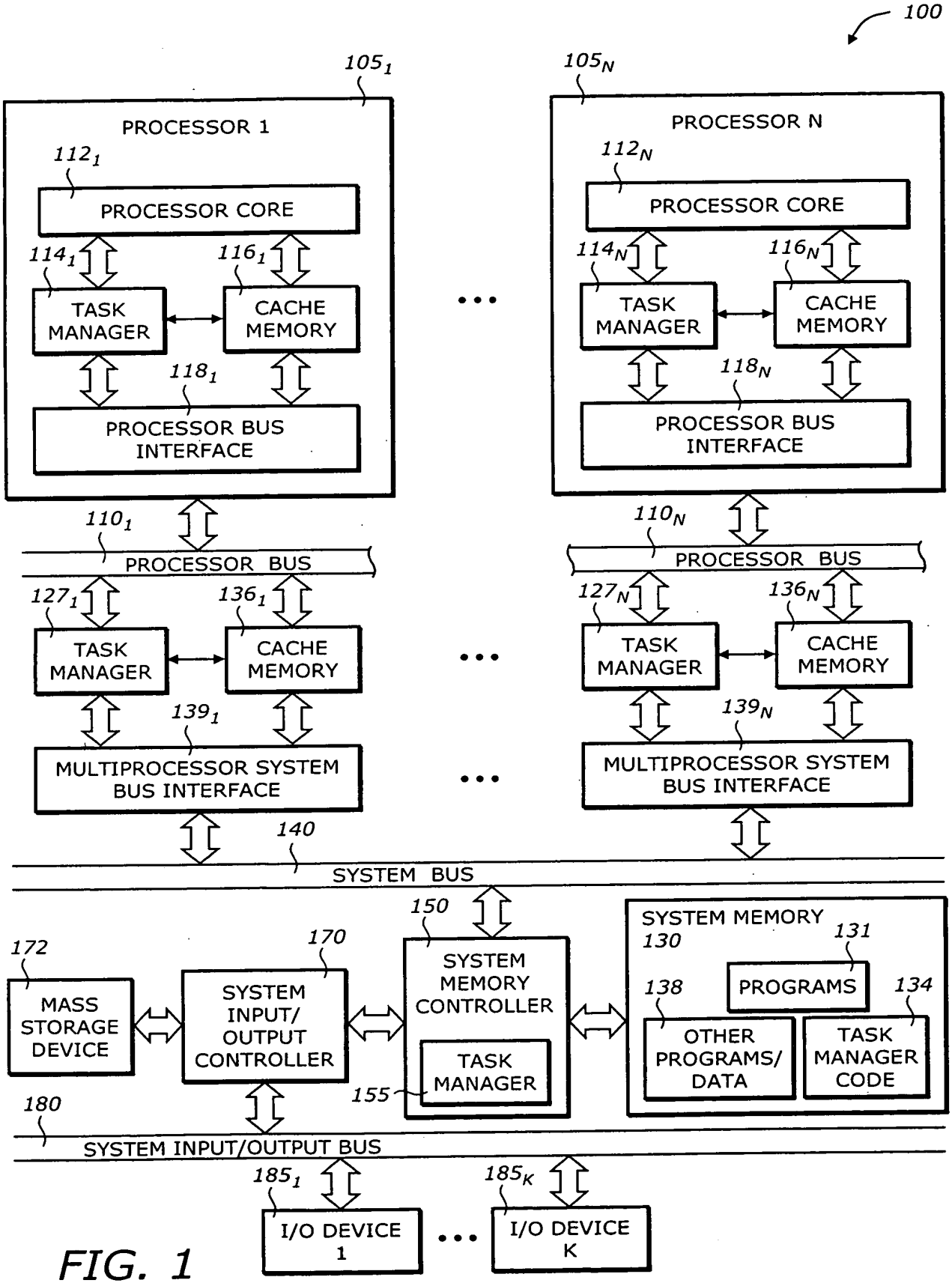
100
105$_1$
PROCESSOR 1
112$_1$
PROCESSOR CORE
114$_1$
116$_1$
TASK MANAGER
CACHE MEMORY
118$_1$
PROCESSOR BUS INTERFACE
105$_N$
PROCESSOR N
112$_N$
PROCESSOR CORE
114$_N$
116$_N$
TASK MANAGER
CACHE MEMORY
118$_N$
PROCESSOR BUS INTERFACE
110$_1$
PROCESSOR BUS
127$_1$
136$_1$
TASK MANAGER
CACHE MEMORY
139$_1$
MULTIPROCESSOR SYSTEM BUS INTERFACE
110$_N$
PROCESSOR BUS
127$_N$
136$_N$
TASK MANAGER
CACHE MEMORY
139$_N$
MULTIPROCESSOR SYSTEM BUS INTERFACE
140
SYSTEM BUS
150
SYSTEM MEMORY CONTROLLER
TASK MANAGER
155
SYSTEM MEMORY
130
131
PROGRAMS
138
134
OTHER PROGRAMS/ DATA
TASK MANAGER CODE
172
MASS STORAGE DEVICE
170
SYSTEM INPUT/ OUTPUT CONTROLLER
180
SYSTEM INPUT/OUTPUT BUS
185$_1$
I/O DEVICE 1
185$_K$
I/O DEVICE K

FIG. 1

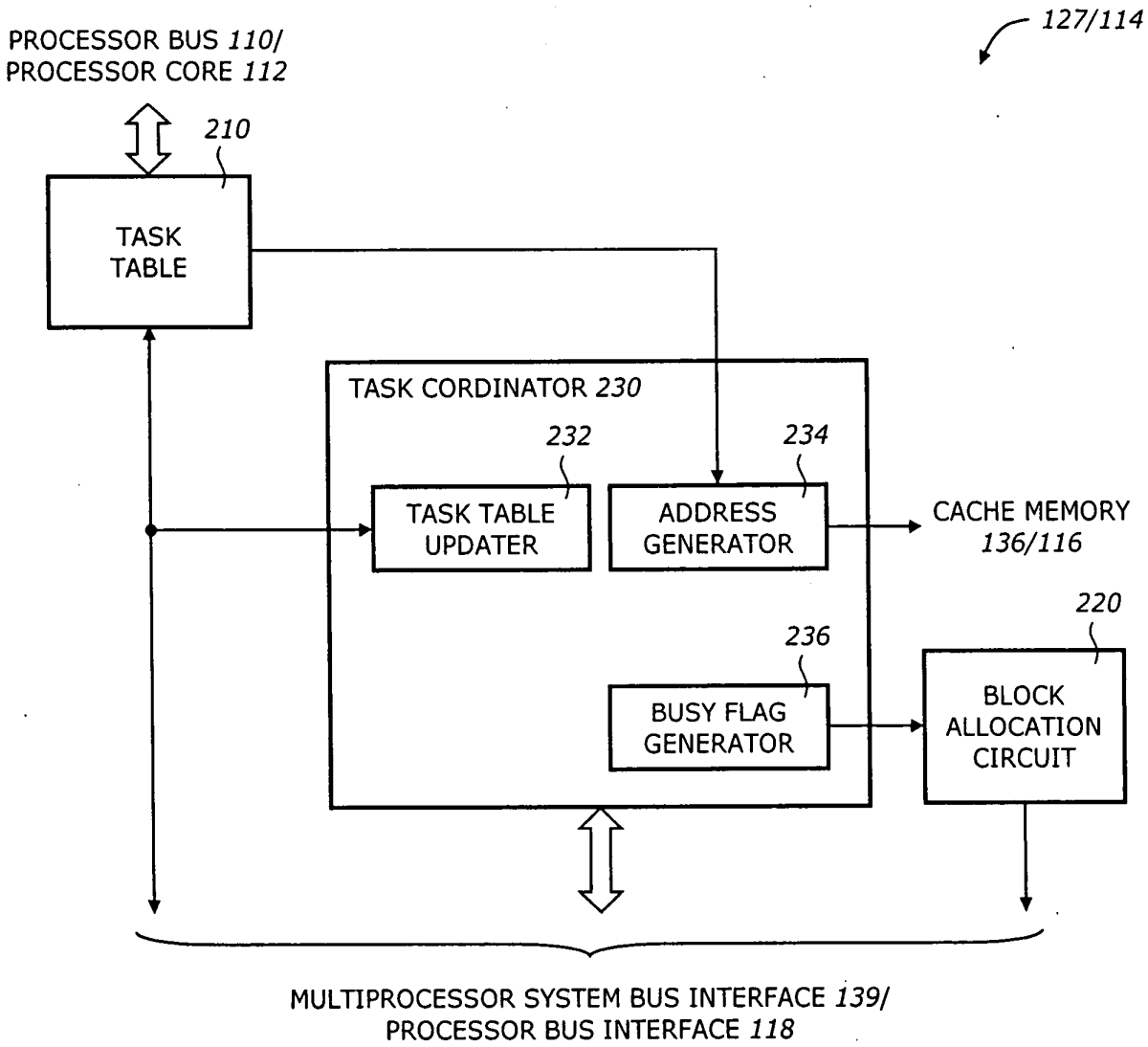
127/114
PROCESSOR BUS 110/
PROCESSOR CORE 112
210
TASK
TABLE
TASK CORDINATOR 230
232
234
TASK TABLE
UPDATER
ADDRESS
GENERATOR
CACHE MEMORY
136/116
220
236
BUSY FLAG
GENERATOR
BLOCK
ALLOCATION
CIRCUIT
MULTIPROCESSOR SYSTEM BUS INTERFACE 139/
PROCESSOR BUS INTERFACE 118

FIG. 2A

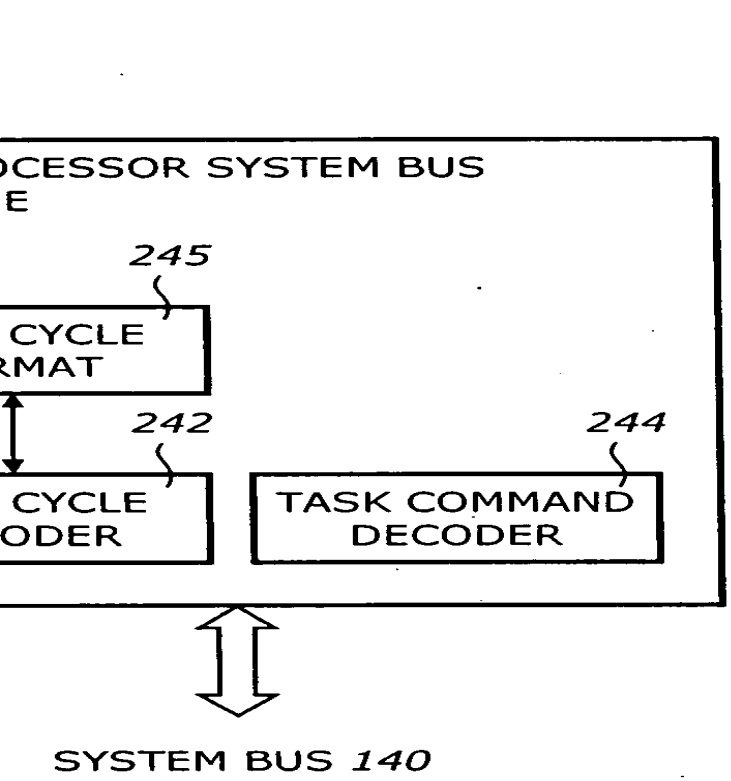
139
OCESSOR SYSTEM BUS
E
245
CYCLE
RMAT
242
CYCLE
ODER
244
TASK COMMAND
DECODER
SYSTEM BUS 140

FIG. 2B

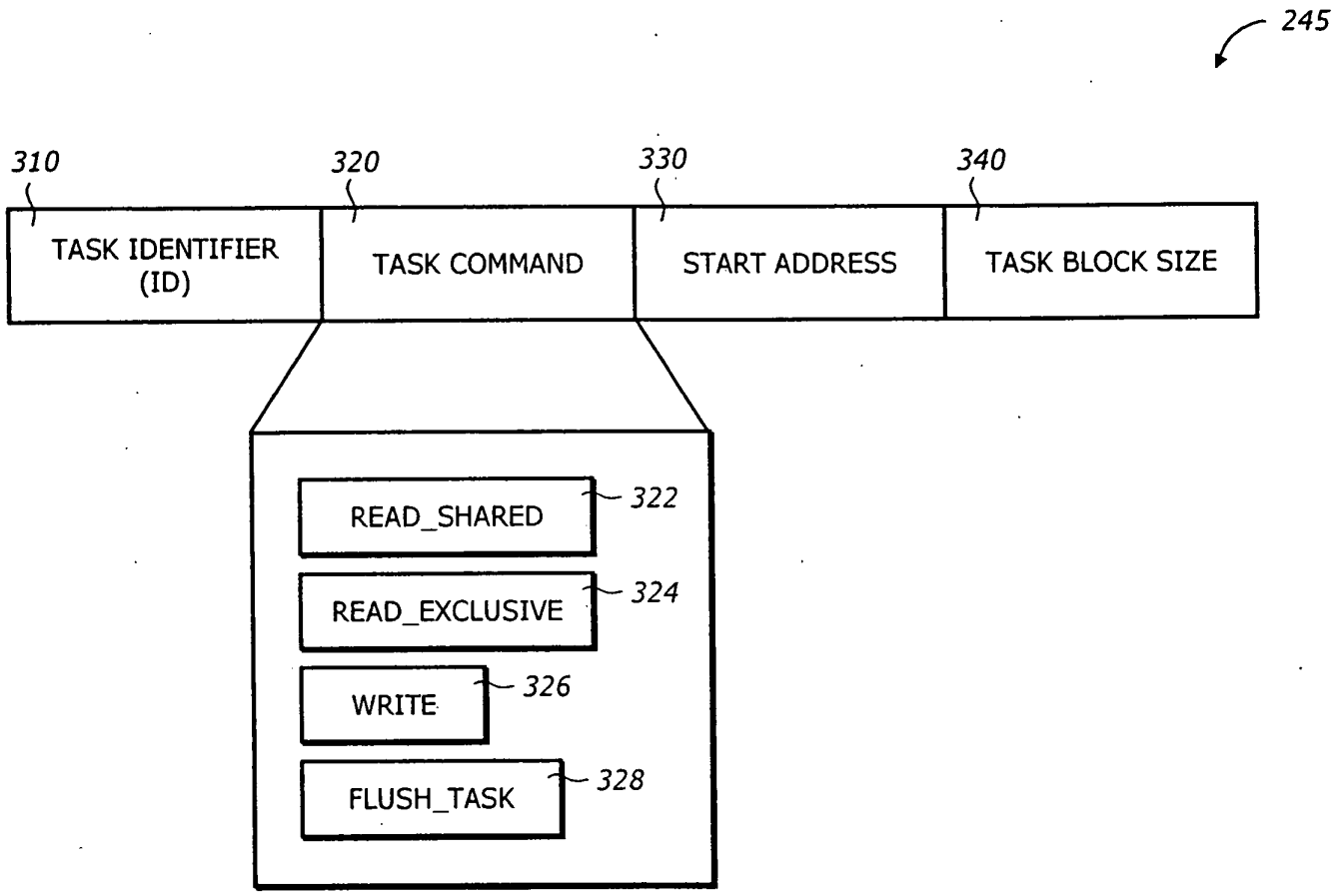
245
310
320
330
340
TASK IDENTIFIER (ID)
TASK COMMAND
START ADDRESS
TASK BLOCK SIZE
READ_SHARED
322
READ_EXCLUSIVE
324
WRITE
326
FLUSH_TASK
328

FIG. 3

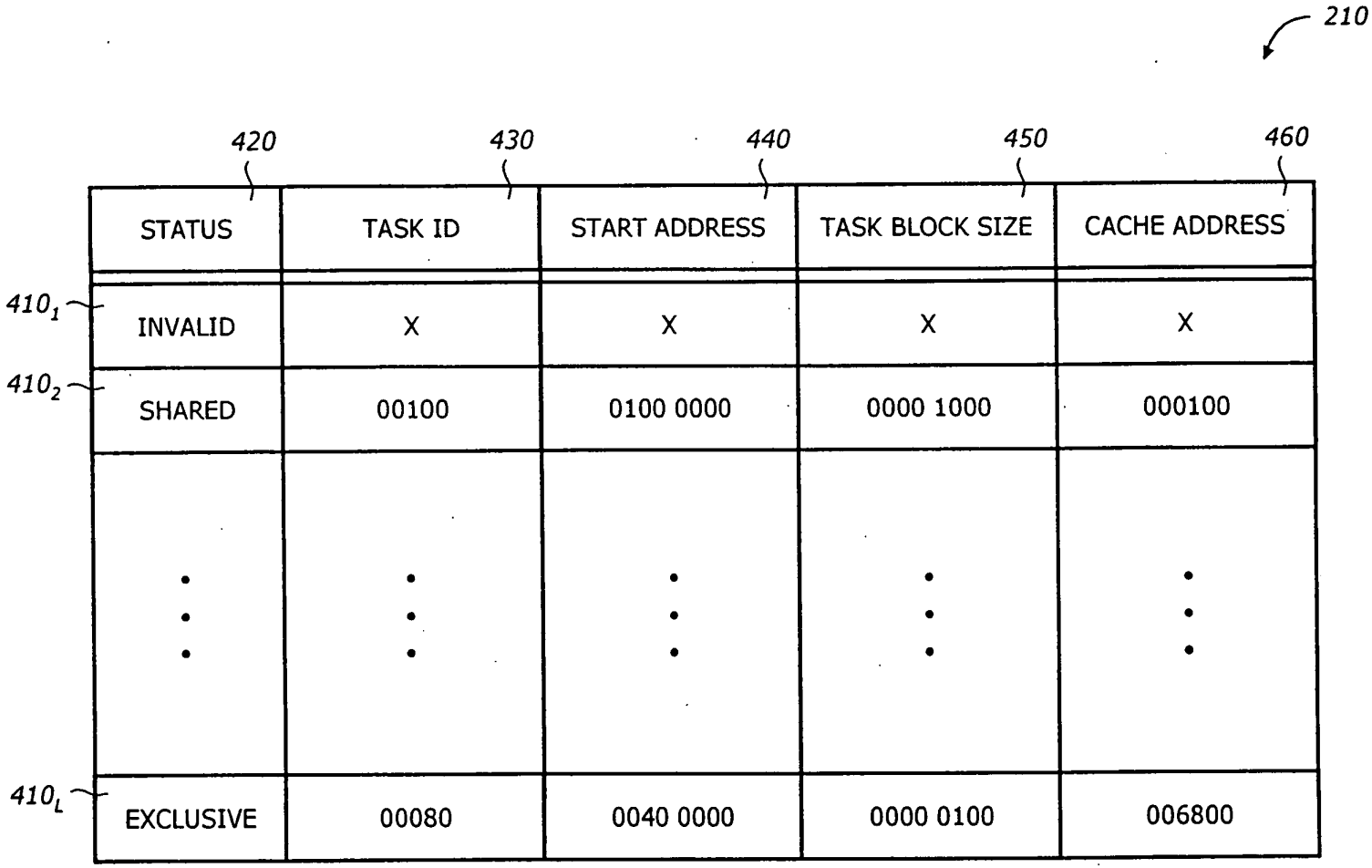
210
420
430
440
450
460
STATUS
TASK ID
START ADDRESS
TASK BLOCK SIZE
CACHE ADDRESS
410_1
INVALID
X
X
X
X
410_2
SHARED
00100
0100 0000
0000 1000
000100
410_L
EXCLUSIVE
00080
0040 0000
0000 0100
006800

FIG. 4

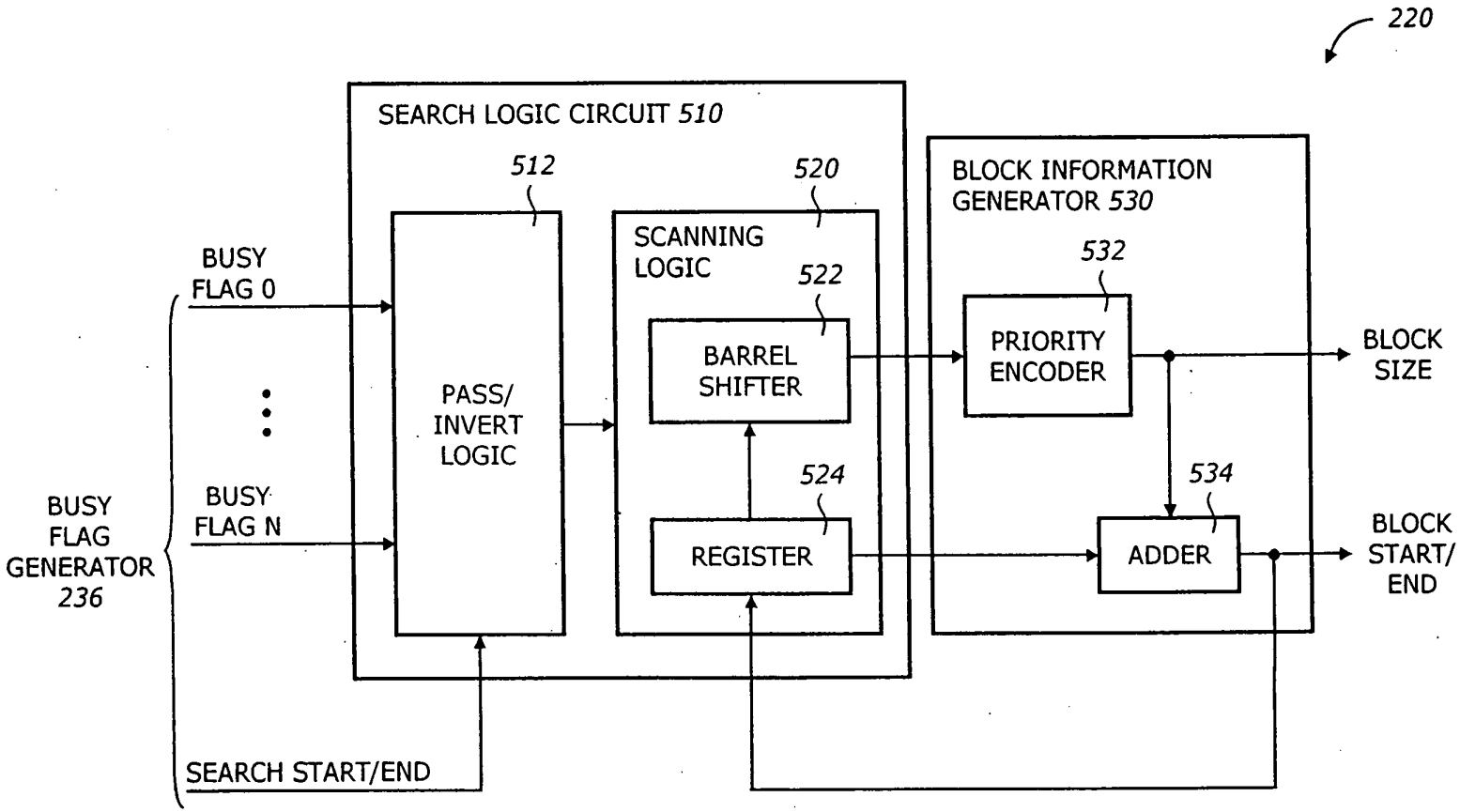
220
SEARCH LOGIC CIRCUIT 510
512
520
BLOCK INFORMATION GENERATOR 530
SCANNING LOGIC
522
532
BUSY FLAG 0
BARREL SHIFTER
PRIORITY ENCODER
BLOCK SIZE
PASS/ INVERT LOGIC
524
534
BUSY FLAG N
BUSY FLAG GENERATOR 236
REGISTER
ADDER
BLOCK START/ END
SEARCH START/END

FIG. 5